Notice of Allowability	Application No.	Applicant(s)	
	09/862,654	TOPHAM, NIGEL PETER	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed 16 March 2006*.

2. ☒ The allowed claim(s) is/are *27-36 and 38-51 renumbered as 1-10 and 11-24*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Pat Burns (Reg. No. 29,367) on 23 May 2006. As per the phone conversation with Mr. Burns on 16 May 2006 and 23 May 2006, the Examiner and Mr. Burns agree that the attached claim amendments do not necessarily change the scope of the claims as examined. The amendments to eliminate the "can" language within the independent claims were to merely clarify the claim language and eliminate possible language discrepancies. The amendments to change "recording medium" to "storage medium" were made to distinguish storage media from signals.

3. The application has been amended as follows: Please see the attached sheets.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AJL
Aimee J. Li
24 May 2006

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

In the Claims:

Please amend claims 27, 36 and 43-51 as follows:

1-26. (Cancelled)

27. (Currently Amended) A method of compressing a program to be executed by a processor which at execution time reads compressed-form instructions stored in a program memory outside the processor, decompresses the compressed-form instructions and caches them in an instruction cache inside the processor prior to issuing the instructions, the processor having a program counter which points directly to addresses in the program memory from which the compressed-form instructions are to be read, the method comprising:

converting a sequence of original instructions of the program into a corresponding sequence of such compressed-form instructions;

assigning such original instructions imaginary addresses according to said sequence thereof, the assigned imaginary addresses determining at said execution time respective locations in said instruction cache into which the instructions read from the program memory are to be loaded after decompression; and

outputting a compressed program comprising the compressed-form instructions together with imaginary address information specifying said assigned imaginary address of at least one said original instruction and storing the compressed program in said program memory so that at said execution time the processor ~~can read~~reads both said compressed-

form instructions and said imaginary address information from program-memory addresses pointed to directly by the program counter and ~~can allocate~~allocates the assigned imaginary addresses to the decompressed instructions based on said imaginary address information and ~~can load~~loads the decompressed instructions into instruction-cache locations determined by the allocated imaginary addresses.

28. (Original) A method as claimed in claim 27, wherein the assigned imaginary addresses are selected so that instructions likely to coexist in the instruction cache at execution time will not be mapped to the same cache block.

29. (Previously presented) A method as claimed in claim 27, wherein the compressed-form instructions are arranged to be stored in said program memory in one or more compressed sections, the compressed-form instructions belonging to each section occupying one cache block of the processor's instruction cache when decompressed, and at least one compressed section also containing imaginary address information relating to the instructions of that section.

30. (Previously presented) A method as claimed in claim 29, wherein said imaginary address information specifies the imaginary address at which a first one of the decompressed instructions corresponding to said at least one compressed section is to be considered to exist when the decompressed instructions are held in said instruction cache.

31. (Original) A method as claimed in claim 29, wherein said imaginary address information is contained in only a first one of said compressed sections to be loaded.

32. (Original) A method as claimed in claim 29, wherein each said compressed section contains imaginary address information relating to the instructions belonging to the section concerned.

33. (Original) A method as claimed in claim 29, wherein the or each said compressed section further contains a decompression key for use by the processor to carry out the decompression of the instructions belonging to said section.

34. (Original) A method as claimed in claim 33, wherein said sequence of original instructions of the program comprises preselected instructions that are not stored explicitly in any said compressed section, and the decompression key of the or each said compressed section identifies the positions at which said preselected instructions exist are to appear in a decompressed sequence of instructions corresponding to the section.

35. (Original) A method as claimed in claim 34, wherein said preselected instructions are "no operation" instructions.

36. (Currently Amended) A computer-readable ~~recordingstorage~~ medium storing a computer program which carries out a method of compressing a processor program to be executed by a processor which at execution time reads compressed-form instructions stored in a program memory outside the processor and caches the decompressed instructions in an instruction cache within the processor prior to issuing them, the processor having a program counter which points directly to addresses in the program memory from which the compressed-form instructions are to be read, the computer program comprising:

a converting portion which converts a sequence of original instructions of the processor program into a corresponding sequence of such compressed-form instructions;

an assigning portion which assigns such original instructions imaginary addresses according to said sequence thereof, the assigned imaginary addresses determining at said execution time respective locations in said instruction cache into which the instructions read from the program memory are to be loaded after decompression; and

an outputting portion which outputs a compressed program comprising the compressed-form instructions together with imaginary address information specifying said assigned imaginary address of at least one said original instruction and storing the compressed program in said program memory so that at said execution time the processor ~~can read~~reads both said compressed-form instructions and said imaginary address information from program-memory addresses pointed to directly by the program counter and ~~can allocate~~allocates the assigned imaginary addresses to the instructions based on said

imaginary address information and ~~can load~~loads the decompressed instructions into instruction-cache locations determined by the allocated imaginary addresses.

37. (Cancelled)

38. (Previously Presented) A processor, for executing instructions of a program stored in compressed form in a program memory, each said compressed-form instruction having an imaginary address at which the instruction is considered to exist when held in decompressed form within the processor, and the program memory also storing imaginary address information from which the imaginary addresses assigned to the compressed-form instructions is derivable, said processor comprising:

a program counter which points directly to addresses in said program memory at which said compressed-form instructions and said imaginary address information are stored;

an instruction cache, having a plurality of cache blocks, each for storing one or more instructions of said program in decompressed form;

an imaginary address deriving unit operable to read the imaginary address information from a program-memory address pointed to directly by the program counter and to derive therefrom the imaginary address of at least a first one of the compressed-form instructions in said program;

a cache loading unit, comprising a decompression section, operable to perform a cache loading operation in which one or more compressed-form instructions are read from program-memory addresses pointed to directly by the program counter and are decompressed and stored in one of said cache blocks of the instruction cache, which cache block is determined by the imaginary addresses of said one or more compressed-form instructions being read from said position in the program memory;

a cache pointer which identifies a location in said instruction cache of an instruction to be fetched for execution;

an instruction fetching unit which fetches an instruction to be executed from the location identified by the cache pointer and which, when a cache miss occurs because the instruction to be fetched is not present in the instruction cache, causes the cache loading unit to perform said cache loading operation; and

an updating unit which updates the program counter and cache pointer in response to the fetching of instructions so as to ensure that said program counter is maintained consistently pointing directly to the address in said program memory at which the instruction to be fetched from the instruction cache is stored in compressed form.

39. (Previously presented) A processor as claimed in claim 38, wherein:

the compressed-form instructions are stored in the program memory in one or more compressed sections, the compressed-form instructions belonging to each section occupying one of said cache blocks when decompressed, and at least one section also

contains imaginary address information relating to the instructions belonging to the section; and

said cache loading unit is operable, in said cache loading operation, to decompress and load into one of said cache blocks one such compressed section stored at the position in the program memory identified by the program counter.

40. (Previously presented) A processor as claimed in claim 39, wherein said imaginary address information of said at least one section specifies the imaginary address at which a first one of the decompressed instructions corresponding to the compressed section is considered to exist when the decompressed instructions are held in one of the cache blocks.

41. (Previously presented) A processor as claimed in claim 39, wherein said imaginary address information is contained in only a first one of said compressed sections to be loaded.

42. (Previously presented) A processor as claimed in claim 39, wherein each said compressed section contains imaginary address information relating to the instructions belonging to the section concerned.

43. (Currently amended) A computer-readable ~~recordingstorage~~ medium storing a compressed program, said compressed program being adapted to be stored in a

program memory of a processor and comprising:

a sequence of compressed-form instructions derived from a corresponding sequence of original instructions, the compressed-form instructions being decompressed by the processor at execution time and the decompressed instructions being cached in an instruction cache inside the processor prior to issuance; and

imaginary address information specifying an imaginary address assigned to at least one of said original instructions, said assigned imaginary address determining a location in said instruction cache into which the instruction is to be loaded, the imaginary address information being present together with the compressed-form instructions in the compressed program so that at execution time, when the compressed program is stored in the program memory, the processor ~~can read~~reads both said compressed-form instructions and said imaginary address information from program-memory addresses pointed to directly by a program counter of the processor and ~~can allocate~~allocates the decompressed instructions to such imaginary addresses based on said imaginary address information and ~~can load~~loads the decompressed instructions into instruction-cache locations determined by the allocated imaginary addresses.

44. (Currently Amended) A computer-readable ~~recordingstorage~~ medium as claimed in claim 43, wherein the assigned imaginary addresses are selected so that instructions likely to coexist in the instruction cache at execution time will not be mapped to the same cache block.

45. (Currently Amended) A computer-readable ~~recordingstorage~~ medium as claimed in claim 43, wherein the compressed-form instructions are arranged to be stored in the said program memory in one or more compressed sections, the compressed-form instructions belonging to each section occupying one cache block of the processor's instruction cache when decompressed, and at least one compressed section also containing imaginary address information relating to the instructions of that section.

46. (Currently Amended) A computer-readable ~~recordingstorage~~ medium as claimed in claim 45, wherein said imaginary address information specifies the imaginary address at which a first one of the decompressed instructions corresponding to said one compressed section is to be considered to exist when the decompressed instructions are held in the same instruction cache.

47. (Currently Amended) A computer-readable ~~recordingstorage~~ medium as claimed in claim 45, wherein said imaginary address information is contained in only a first one of the said compressed sections to be loaded.

48. (Currently Amended) A computer-readable ~~recordingstorage~~ medium as claimed in claim 45, wherein each said compressed section contains imaginary address information relating to the instructions belonging to the section concerned.

49. (Currently Amended) A computer-readable ~~recordingstorage~~ medium as claimed in claim 45, wherein the or each said compressed section further contains a decompression key for use by the processor to carry out the decompression of the instructions belonging to the said section.

50. (Currently Amended) A computer-readable ~~recordingstorage~~ medium as claimed in claim 49, wherein said corresponding sequence of original instructions includes preselected instructions that are not stored explicitly in any said compressed section, and the decompression key of the or each said compressed section identifies the positions at which said preselected instructions exist are to appear in a decompressed sequence of instructions corresponding to the section.

51. (Currently Amended) A computer-readable ~~recordingstorage~~ medium as claimed in claim 50, wherein said preselected instructions are "no operation" instructions.